PHASE DETECTOR AND METHOD HAVING HYSTERESIS CHARACTERISTICS

ABSTRACT OF THE DISCLOSURE

A phase detector generates a first output signal if a feedback clock signal leads a reference clock signal by more than a first time. The phase detector generates a second output signal if the feedback clock signal lags the reference clock signal by more than a second time. If the feedback clock signal either leads the reference clock signal by less than the first time or lags the reference clock signal by less than the second time, neither output signal is generated. The phase detector may be used in a delay-lock loop in which the first and second output signals increase or decrease a delay of the reference clock signal by respective first and second delay increments. In such case, the each of the first and second delay increments should be less than the sum of the first and second times.